A DYNAMICALLY RECONFIGURABLE SIGNAL PROCESSING APPARATUS AND METHOD FOR USE IN A HIGH SPEED DIGITAL COMMUNICATION SYSTEM

The present invention is generally related to signal processing, and more particularly to a dynamically reconfigurable signal processor for performing different signal processing functions in real-time or near-real time.

Wireless digital communication systems require a number of channel modulation and demodulation functions to be performed for the transmission and reception of digital data over such a network. The modulation and demodulation functions typically consist of signal processing functions, which are performed in the digital domain using well known methods and techniques of digital signal processing (DSP). In high-bandwidth radio-frequency systems, the sampling rates required for DSP are very high, so that these functions have traditionally been performed using custom, dedicated digital logic hardware (i.e., a conventional DSP computer processor is not capable of operating at the data rates required to support such high sampling rates).

More recently, some computer architectures that are capable of performing DSP functions at the required sampling rates have been developed, and are known in the art as "software radios". These so-called software-radios typically consist of parallel processing arrays having a substantial number of small but very fast computer processors operating in concert such that each processor performs a portion of the required signal processing thus allowing the array to perform the necessary DSP functions at the required sampling rate. Such architectures can be readily configured to operate in any of a plurality of communication schemes which utilize a wide variety of modulation and demodulation methods simply by programming the processor(s) with the requisite software to perform the appropriate function(s).

The term software radio is used to describe radios that provide software control of a variety of modulation techniques, wide-band or narrow-band operation, communications security functions (such as hopping), and waveform requirements of current and evolving standards over a broad frequency range.

U.S. Pat. No. 6,181,734 issued to Palermo discloses a software radio that operates in accordance with a software program that runs on a generic radio platform. Interoperable waveform modes are added as software applications in a manner similar to adding applications to a personal computer.

Another example of this type of device is described in U.S. Pat. No. 6,091,715, to Vucetic, for a Hybrid Radio Transceiver. Vucetic indicates that this type of radio transceiver provides for software-defined parameters to achieve flexibility in modulation and protocol types.

None of the above patents or existing technology addresses the need for a software radio that can be dynamically reprogrammed in real-time or near real-time to perform different signal processing functions responsive to a detected change of system state.

The present invention provides a dynamically re-configurable digital signal processing device for performing, in real-time or near real-time, different digital signal processing functions responsive to changes in a system state. The invention is also directed at implementing the digital signal processing device in a reduced silicon surface area.

In accordance with one aspect of the present invention, a system of the invention includes at least a system controller, an array controller and an array-type processor. The array-type processor includes a plurality of data processing elements, each data processing element further including a dedicated program memory for storing a portion of signal processing function code data for executing a digital signal processing function in response to a change of system state. The different signal processing functions can include, for example, FFT processing, correlation, digital filtering and the like.

According to one embodiment of the present invention, the signal processing device may be dynamically re-configured in real time or in near real time by downloading signal processing function code data from an external memory to be stored in the dedicated program memories of respective ones of the data processing elements for execution therein.

According to another embodiment of the invention, the dedicated memory of each data processing element may be configured as a plurality of memory banks. The plurality

of memory banks are pre-loaded with signal processing function code data associated with different digital signal processing functions required at various stages of a high speed digital communication system. The array-type processor is configured to switchably select, in real time or in near real time, the memory bank storing the signal processing function required in response to a change of system state. In this manner, the signal processing function code data is instantaneously available for execution by the array type processor. In this embodiment, the need to download the signal processing function code data from an external memory is obviated.

In accordance with another aspect of the invention, in a digital signal processing device, a method for reconfiguring the device in real-time or in near real-time to perform different signal processing functions as needed, comprises the acts of: (i) receiving input digital information at said network node; (ii) detecting a change of state in said network node; (iii) identifying at least one signal processing function to be performed responsive to said detected change of state in said network node; and (iv) dynamically reconfiguring, in real time or in near real-time, the signal processing device to perform said at least one signal processing function, responsive to said detected change of state.

Advantageously, the signal processing device of the present invention provides equivalent functionality as that provided by a plurality of dedicated hardware and/or software signal processing devices of the prior art using fewer resources. Moreover, it is to be appreciated that the ability to dynamically reprogram the signal processing device of the invention to perform different signal processing functions leads to a reduced silicon surface area with respect to prior art circuits. Design productivity is improved as a result.

The foregoing features of the present invention will become more readily apparent and may be understood by referring to the following detailed description of an illustrative embodiment of the present invention, taken in conjunction with the accompanying drawings, where

FIG. 1a is a prior art system diagram illustrating a cellular system within which the present invention may be deployed;

FIG. 2 is a block diagram generally illustrating the structure of a wireless network

node constructed according to the prior art;

FIG. 3 is a more detailed illustration of signal processing unit 158c of FIG. 2 constructed in accordance with the prior art;

FIG. 4 is a more detailed illustration of signal processing unit 158c of FIG. 2 constructed in accordance an embodiment of the invention; and

FIG. 5 is a more detailed illustration of signal processing unit 158c of FIG. 2 constructed in accordance with another embodiment of the invention.

The present invention generally provides techniques for dynamically re-configuring a signal processing apparatus to perform different signal processing functions in a high-speed digital communication system responsive to different criteria, including, but not exclusive to, detected changes of in the channel and/or system data of a network node incorporating the signal processing apparatus.

The invention is illustrated in conjunction with an exemplary architecture for processing data for transmission through a network. The exemplary system includes a network processor array configured as a two-dimensional array, e.g., (MxN, NxN). It should be understood, however, that the invention is more generally applicable to any processor configuration in which it is desirable to provide signal processing functionality through the use of dynamic re-configurability.

In accordance with embodiments of the invention, the signal processing apparatus of the invention can be dynamically reprogrammed, in real time or in near real time, to perform a signal processing function required in response to a detected change of system state. This is in contrast to the prior art, in which resources, in the form of either dedicated hardware or software signal processors, are constructed in such a way as to be dedicated (i.e., hardwired) to each digital signal processing function to be performed.

The present invention has particular, but not exclusive, application to various aspects of wireless data networking. It is to be appreciated, however, that the present invention is not limited to this or any particular data networking application.

In the area of wireless data networking, a network node must be capable of performing a number of different digital communication functions, depending upon the specific network standard. In many cases, however, only one digital communication function, i.e., the currently active function, is in use at any particular point in time.

Accordingly, the signal processing apparatus of the invention need only be configured to perform the digital processing function needed at that time. For example, it is well known that the IEEE 802.11a networking standard supports four different modulation methods, i.e., BPSK, QPSK, 16 and 64 level QAM. In prior art approach of providing dedicated hardware/software for processing data in accordance with each standard is obviated with the signal processing device of the invention. In particular, the reconfigurable signal processing device of the invention may be dynamically configured and re-configured in real-time or in near real-time at run-time to operate in accordance with each of the afore-mentioned modulation methods. The required modulation method being detectable using rate information transmitted in the packet header, which is typically transmitted following the preamble. In this manner, the reconfigurable apparatus of the invention precludes the need for dedicated hardware/software for each of the four modulation methods.

FIG. 1 is a system diagram illustrating an exemplary cellular system 10 within which the present invention may be deployed. The cellular system includes a plurality of base stations 102, 104, 106, 108, 110, and 112 that service wireless communications within respective cells, or sectors. The cellular system services wireless communications for a plurality of wireless subscriber units. These wireless subscriber units include wireless handsets 114, 118, 120, and 126, mobile computers 124 and 128, and desktop computers 116 and 122. During normal operations, each of these subscriber units communicates with one or more base stations during handoff among the base stations 102 through 112. Each of the subscriber units 114 through 128 and base stations 102 through 112 include signal processing apparatus constructed according to the present invention, as will be described below.

FIG. 2 is a block diagram generally illustrating the structure of a wireless network node 100 constructed in accordance with the prior art. The general structure of wireless device 100 will be present in any of the subscriber units 114 through 128 and base stations 102 through 112 illustrated in FIG. 1. Wireless device 100 includes an antenna 160, an RF front end 152, a signal processing front end 154 including conventional signal processing components 158A, 158B, 158C. Wireless device 100 also includes a plurality of host device components 160 that service all requirements of wireless device 100 except for the RF requirements 152 and front end 154 signal processing requirements.

FIG. 3 is a more detailed illustration of signal processing unit 158C of FIG. 2 constructed in accordance with the prior art. The signal processing apparatus 158C is comprised of an input data interface 110, for receiving digital input data 9. The input data interface 110 buffers the digital input data 9 in data buffer 23 and outputs buffered digital data 11 to be provided to a processor array 120. The processor array 120 is embodied as a collection of processing elements 122 in a matrix configuration. The processing elements 122 are preferably configured as an array of primitive configurable processors designed for high throughput reconfigurable signal processing. Each processor retains a primitive instruction set, minimum local storage (a program memory 124), and exchanges data with adjacent processors using nearest neighbor communication. Additional details regarding array processing are described in, for example, G. Burns and K. Vaidyanathan, "Array Processing For Channel Equalization", Philips Research USA, which is incorporated by reference herein. The array of processing elements 122 are configured to perform different signal processing functions by loading appropriate digital processing function software into each of the respective memory elements 124 at the appropriate time. Software for a particular signal processing function may be loaded into the processor array 120 from a memory unit 130, under control of the array controller 140.

The signal processing apparatus 158C further includes an output data interface 160 which receives processed output data 15 processed by processor array 120 and buffers the processed output data in data buffer 25. The buffered output data 13 is output to host device components 160 as needed.

With reference now to FIGS. 4 and 5, preferred embodiments of the invention are illustrated and described.

FIG. 4 is a detailed view of the signal processing unit 158C of FIG. 3 according to one embodiment of the invention. As shown in figure 4, the signal processing unit 158C includes the elements described above in FIG. 3, and additionally includes system controller 170.

The system controller 170 is shown to include a first input 173 labeled "Input data", coupled to an output of the input data interface 110, a second input 171 labeled "channel/system" data coupled to a source of channel/system data, a third input 175

labeled "output data" coupled to an output of the output data interface 160 and a single output labeled "re-configuration request" 177 coupled to an input of the array controller 140. It is to be understood that different embodiments of the invention may utilize different combinations of the inputs and outputs described above.

System controller 170 determines the present state of the network node 100 according to one or more of the following: (1) channel and system data received via the "Channel/System data" input 171 (2) protocols defined by the prevailing network standard (e.g., IEEE 802.11b) under which the network node 100 is operating, (3) input data 9 received via the "Input data" input 173, and (4) output data fed back via the "Output data" input 175. The present state of the network node 100 in turn dictates the signal processing function to be performed by the signal processing unit 158c at any point in time.

The array controller 140 is shown coupled to an external memory 130 via data line 180 for retrieving signal processing function code from the memory 130 in response to a "reconfiguration request" command 177 output from the system controller 170. An output of array controller 140 is shown coupled to an input of the processor array 120 via data line 181 for outputting the signal processing function code from the external memory 130 to the processor array 120.

In operation, when the system controller 170 detects a change in the system state in the network node 100 in accordance with one or more of the four afore-mentioned conditions recited above, it issues a "re-configuration request" command 177 to the array controller 140. The array controller responds to the "re-configuration request" command 177 by downloading appropriate signal processing function software pre-stored in the external memory 130. The external memory 130 preferably stores signal processing function software for each of the digital signal processing functions to be performed by the network node 100. The stored signal processing functions could include, for example, functions associated with FFT processing, correlation, digital filtering and so on. It is noted that the external memory 130 is preferably a non-volatile memory or other suitable memory.

Responsive to the "re-configuration request" command 177, the signal processing function software is downloaded from the external memory 130 to the processor array

120 to carry out the signal processing function required at that point in time. In certain cases, more than one signal processing function may be required to be carried out at any point in time. It is to be appreciated that the simultaneous performance of multiple signal processing functions requires that portions of the processor array 120 are dedicated to particular signal processing functions. It should also be appreciated that in other cases, the signal processing functions to be performed may require less than the total processing capability of the processor array 120, in which case certain processing elements 122 in the array 120 may remain idle.

In the present embodiment, the various processing elements 122 are loaded via dedicated lines 180, 181, which may be embodied as a single multiplexed data bus into the program memories 124 of the processing elements 122. Those of skill in the art can appreciate that the process of loading software into the program memories 124 over a single multiplexed bus 180, 181must be performed at a sufficiently high speed to comply with the timing requirements of the prevailing network standard under which the network node 100 is operating. Because the allotted time in some cases, can be very short, it is necessary that the software loading mechanism be fast. To insure proper synchronization, in certain embodiments, such as the one shown in FIGS. 3 - 5, input and output data is shown to be buffered in the input 23 and output 25 data buffers.

Once the software pertaining to a presently required signal processing function is loaded into the respective program memories 124, the signal processing function is executed by the processor 120 yielding processed output data 15 to be supplied to the output data interface 160.

In accordance with another embodiment of the invention, the time in which the processor array 120 is re-configured may be improved by associating multiple (i.e., two or more) program memories 125a- 125n (see FIG. 5) with each processing element 122 in the processor array 120 to pre-store signal processing function code data for multiple signal processing functions. In this manner, the need to download the signal processing function code data from an external memory, such as external memory 130, is obviated.

FIG. 5 is a more detailed view of the signal processing unit 158C of FIG. 3 according to the present embodiment. As shown in FIG. 5, the signal processing unit 158C includes those elements described above in FIG. 4. In addition, FIG. 5 further

includes multiple dedicated program memory elements 125a – 125n associated with each processing element 122. The program memory elements 125a – 125n are bank selectable by the array controller 140. That is, the array controller 140 is capable of switching from one program memory element in the bank to another at any point in time.

The multiple memory banks 125a – 125n associated with each processing element 122 are preferably pre-loaded in advance, where each memory bank stores signal processing function code data for a particular signal processing function. For example, a first program memory bank 125a may be pre-loaded with signal processing function code data associated with a correlation signal processing function and a second program memory bank 125b may be pre-loaded with signal processing function code data associated with an FFT signal processing function.

A key feature of this embodiment, is that the signal processing function code which define corresponding signal processing functions are pre-stored in the respective program memories 125a-n for virtually instantaneous access upon demand without having to retrieve the signal processing function code from an external memory 130, thus providing significant performance advantages in terms of execution time and speed.

In operation, upon detecting a change of state, the system controller 170 directs the array controller 140 to switchably select one of the pre-loaded program memory banks, e.g., bank 125j, storing the signal processing function code associated with a signal processing function to be performed in response to the detected change of state.

The capability for switch selecting memory banks 125a-n provides virtually instantaneous access to the required signal processing function code. The time delay associated with downloading function code from an external memory 130 is obviated. Accordingly, reconfiguration of the respective processor elements 122 can be performed within sufficient time to meet the requirements of all well-known network standards.

It is to be appreciated that, in those cases where it is known before hand that the time allotted for reconfiguring the processor array 120 is sufficiently long, the first embodiment may be utilized. That is, in those cases in which it is known that there is sufficient time to dynamically download the required function code from the external memory 130, the method of the first embodiment will suffice.

It should also be appreciated that in each of the described embodiments herein, the processor array 120 may be addressed individually, in processor groups, or as an entire array. In other words, if two signal processing functions are to be performed simultaneously in the processor array 120, a first signal processing function, e.g., function A, can be performed in a first subset of processing elements 122 and a second function, function B, can be simultaneously performed in a second subset of processing elements 122.

Exemplary Application

The IEEE 802.11 wireless LAN standard represents an important exemplary application of the invention. However, it should be noted that the invention is not limited to this standard and can be employed in many different communication standards.

According to the 802.11 standard, a "preamble" is transmitted before the "payload" (actual data) is transmitted. The signal processing requirements for the "preamble" portion, required for receiver synchronization, can be quite different from that required for the payload portion, used for data reception. The two operations occur at mutually-exclusive times (i.e., at any given time, either preamble or payload is being received, but never both). Furthermore, a node is either receiving or transmitting data at a given time, but never at the same time. The signal processing device of the invention can be configured to perform the preamble processing at the appropriate time, and thereafter, dynamically reconfigured, in real time or in near real time, to perform the payload (data transmission) processing at the appropriate time. For example, the signal processing apparatus can be initially configured as a correlator when required to process the preamble portion, and subsequently re-programmed as an FFT when required to process the payload data. It is to be appreciated that by virtue of dynamically re-configuring the signal processing apparatus of the invention in real time or near real time to perform the particular signal processing function required at any point in time, the available radio resources are optimized.

It will be apparent to those of skill in the art that the disclosed apparatus and method has numerous applications in the area of wireless data networking.

Although this invention has been described with reference to particular embodiments, it will be appreciated that many variations will be resorted to without departing from the spirit and scope of this invention as set forth in the appended claims. The specification and drawings are accordingly to be regarded in an illustrative manner and are not intended to limit the scope of the appended claims.

In interpreting the appended claims, it should be understood that:

a) the word "comprising" does not exclude the presence of other elements or acts than those listed in a given claim;

b) the word "a" or "an" preceding an element does not exclude the presence of a plurality of such elements;

c) any reference signs in the claims do not limit their scope;

d) several "means" may be represented by the same item or hardware or software implemented structure or function; and

e) each of the disclosed elements may be comprised of hardware portions (e.g., discrete electronic circuitry), software portions (e.g., computer programming), or any combination thereof.